DESCRIPTION/SPECIFICATIONS/STATEMENT OF WORK

TASK ORDER (TO) STATEMENT OF WORK (SOW)
TITLE: BACK-END-OF-LINE (BEOL) 4H-SiC SILICON CARBIDE (SiC) INTEGRATED CIRCUIT PROCESSING ON 100 mm DIAMETER SiC WAFERS

1. **BACKGROUND**
The scope of this work is described online at https://www1.grc.nasa.gov/research-and-engineering/silicon-carbide-electronics-and-sensors/. NASA is developing extreme environment-durable integrated circuits (ICs) to advance the capabilities of a variety of planned NASA missions including Venus landers. Towards this end, NASA Glenn Research Center is seeking prototype fabrication of increasingly capable silicon carbide (SiC) junction field effect transistor (JFET) ICs. In particular, this procurement is seeking fabrication of particular integrated SiC device structures (JFETs and resistors) via a particular fabrication process flow to the following specifications on NASA-provided 100 mm diameter 4H-SiC epilayered wafers using NASA-provided device-layout design files.

2. **SCOPE**
This procurement is seeking fabrication of specific integrated SiC device structures (JFETs and resistors) via a particular fabrication process flow to the following specifications on NASA-provided partially processed 100 mm diameter 4H-SiC epilayered wafers using NASA-provided device-layout design files. After the SiC device structures of the following statement of work are completed, the wafers will be delivered back to NASA for additional processing of bondpads and the back-side contact that will complete the formation of integrated circuits needed for NASA missions. The resulting IC chips produced will be used to implement prototype extreme-environment electronic systems and demonstrations. A technical primer (overview) of the IC technology being implemented is online at https://www1.grc.nasa.gov/research-and-engineering/silicon-carbide-electronics-and-sensors/jfet-ic-tech-guide/ .

3. **OBJECTIVES**
The responsive bids for this procurement shall include information that will enable NASA to evaluate which prospective bidders possess the relevant semiconductor device fabrication equipment, facilities, competence to successfully execute the Statement of Work within reasonable cost and schedule.

4. **TASK DESCRIPTION AND REQUIREMENTS**
In accordance with the following specifications including semiconductor microfabrication process flow and device structure cross-sectional diagrams/depictions, the Contractor shall fabricate and deliver to NASA, the contact metal, two levels of patterned $TaSi_2$ and three dielectrics so as to interconnect 4H-SiC JFET and resistor (JFET-R) device structures arrayed across the silicon-face surface area of six (6) NASA-provided 100 mm diameter 4H-SiC wafers provided by NASA according to NASA design files to be provided to the contractor in Graphic Database System II (GDS) format. Information regarding the layers, layout feature dimensions and layout rules for device pattern features to be present in the NASA design files is available online at https://www1.grc.nasa.gov/research-and-engineering/silicon-carbide-electronics-and-sensors/jfet-ic-tech-guide/ .

The Contractor shall perform the following tasks:
The 4H-SiC JFET-R device structures delivered to NASA by the contractor shall conform to the salient features shown in Figure 1 schematic depiction of the (a) cross-section and (b) top view of an example integrated 4H-SiC JFET-R device to be implemented with the NASA-provided partially processed 4H-SiC wafer:

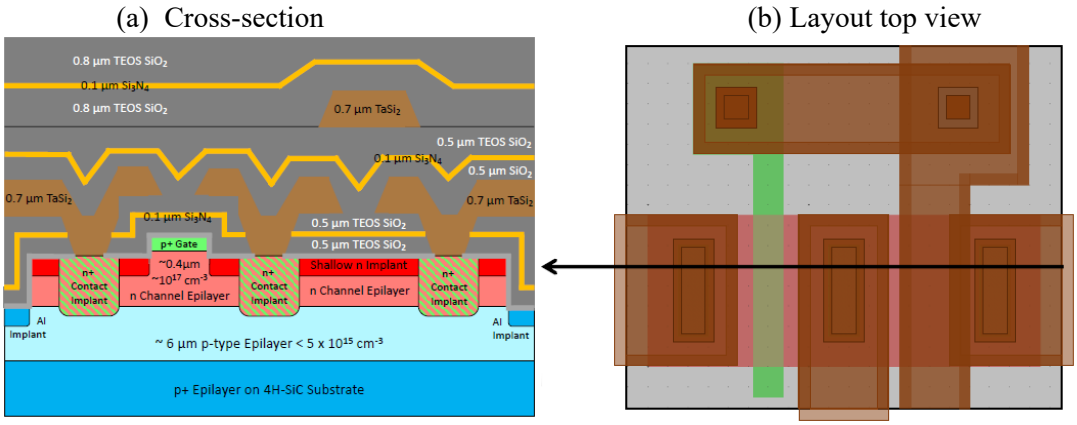

Figure 1: Simplified schematic illustration detail of example 4H-SiC JFET and resistor (JFET-R) devices as they will be interconnected at the conclusion of all tasks.

The contractor shall fabricate the above depicted device structure using the following sequence order of major semiconductor device processing steps (i.e., "Major Steps") described and illustrated as follows starting from the Figure 2 simplified schematic depiction of (illustrating a small closeup portion of) the NASA-provided front-end-of-line (FEOL) completed 4H-SiC wafers:

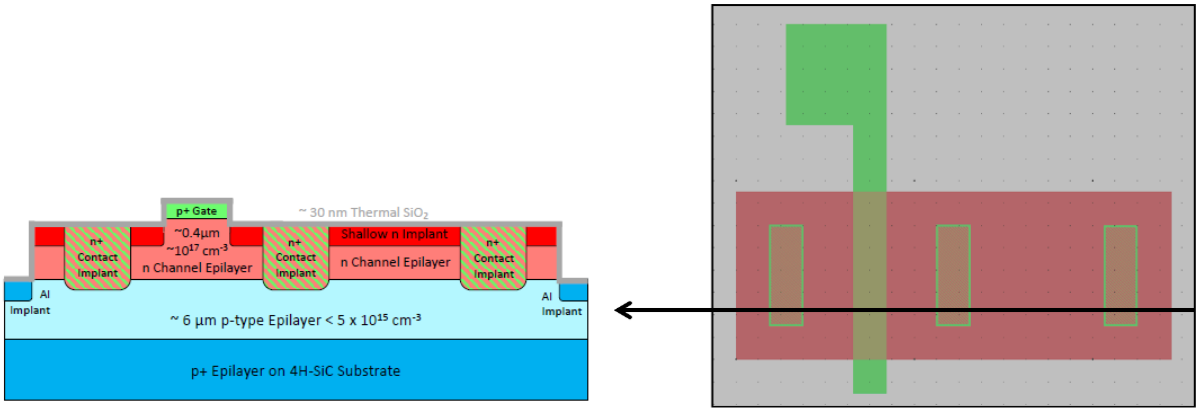

Figure 2: Simplified schematic cross-section of SiC JFET and SiC resistor structures on the wafers NASA will provide. **<u>This is the BEOL starting point</u>**.

After the completion of each major step listed below, the contractor shall E-mail required data/documentation listed in each major step to the NASA's Technical Monitor (TM) so that NASA can verify and quantify contractor progress and workmanship during the performance of this Statement of Work. The contractor shall additionally also explicitly note any and all off-nominal observations and processing detected and provide accompanying relevant data. Examples of off-nominal observations include larger than 10% non-uniformities in deposited film thicknesses, or etch depths, de-lamination, buckling, or peeling of metal films, cracking or peeling of dielectric films, etc. in any wafer regions farther than 4 mm from a wafer edge.

Major Step 1, Deposit first 1.1µm-thick 3-layer dielectric stack: The contactor shall implement further processing consisting of Parts A-C that results in intermediary device structure depicted in Figure 3 as follows:

Part A: The contractor shall deposit of 0.5 µm ± 0.05 µm thickness of SiO_2 over the entire wafer top surface. The SiO_2 film shall be deposited by Low Pressure Chemical Vapor Deposition (hereafter abbreviated as LPCVD) using tetraethyl orthosilicate (hereafter abbreviated as TEOS) at a deposition temperature of 720 °C. The resulting SiO_2 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

Part B: The contractor shall deposit of 0.1 µm ± 0.01 µm thickness of stoichiometric Si_3N_4 over the entire wafer top surface. The Si_3N_4 film shall be deposited by LPCVD at a deposition temperature of 720 °C. The resulting Si_3N_4 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

Part C: The contractor shall deposit of 0.5 µm ± 0.05 µm thickness of SiO_2 over the entire wafer top surface. The SiO_2 film shall be deposited by LPCVD using TEOS at a deposition temperature of 720 °C. The resulting SiO_2 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 1: Optical microscope images showing a few SiC JFET and resistor mesas.

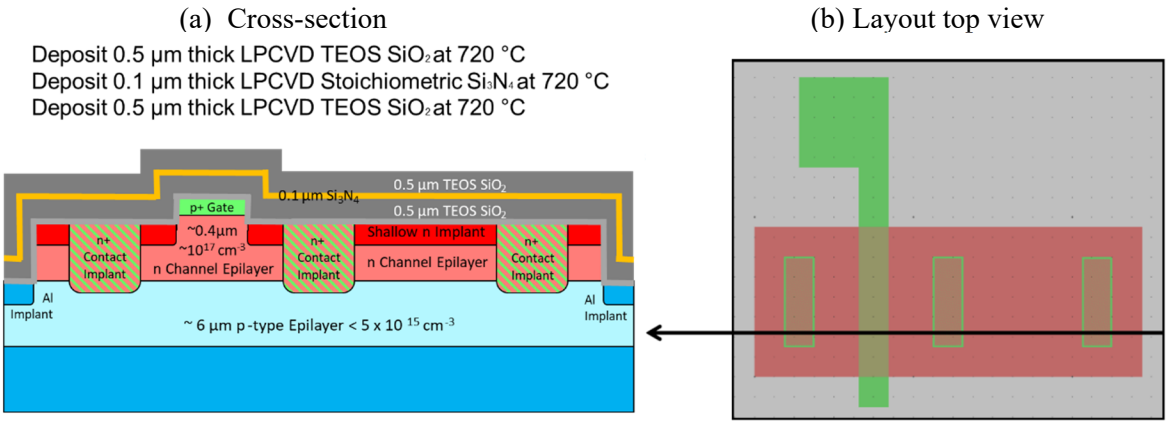

Figure 3: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 1 processing.

Major Step 2, Photolithography and etching of Via1: The contactor shall implement further processing consisting of Parts A and B that results in intermediary device structure depicted in Figure 4 as follows:

Part A: Implement photolithographic process patterning of a suitable photoresist etch masking material that reproduces the "Via1" layer pattern in the NASA-provided GDS design file onto the wafer. The NASA-provided design file for this Via1 pattern has a minimum feature width of 3 µm and a minimum feature separation spacing distance of 6 µm. This Via1 etch mask shall be deposited and patterned in a manner that aligns to and covers p+ gate features produced on the wafer during to within 0.2 µm. The reproduced and resulting "Via1" etch masking pattern defined onto the wafer shall not laterally deviate from the NASA-provided design file dimensions by more than 0.2 µm for 999 out of every 1000 3 µm x 3 µm Via1 features patterned into the photoresist. The thickness and composition of the photoresist Via1 mask shall be sufficiently durable that it can remain on the wafer and provide for:

(i) Dry etch removal of the entire thickness of dielectrics as specified in Part B.

(ii) Photoresist remaining following dry etch described in Part B is sufficient in thickness and sidewall profile that facilitates liftoff patterning of sputtered Ti + $TaSi_2$ contact plug as specified in Major Step 3.

Part B: Implement etch removal of the first 1.1 µm-thick 3-layer dielectric stack (deposited in Major Step 1) plus removal of entire thickness of high-quality thermal SiO_2 layer #3 of 30 nm ± 10 nm (formed in Major Step C-5, Part E) wherein dielectric removal only occurs in those lateral 3 µm x 3 µm regions where patterned photoresist is not residing prior to the start of the dry etch. In each 3 µm x 3 µm region not protected by photoresist, this etch removal of dielectric shall remove all dielectric to form an exposed SiC surface region laterally larger than 1.7 µm x 1.7 µm, but this etch removal of dielectric shall not remove/etch more than 10 nm of depth into the SiC. This etch removal of dielectric shall be implemented by plasma-based dry etching.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 2:

1. Optical microscope images showing a few SiC JFET and resistor mesas recorded after Part A prior to Part B.
2. Optical microscope images showing a few SiC JFET and resistor mesas recorded after Part B.

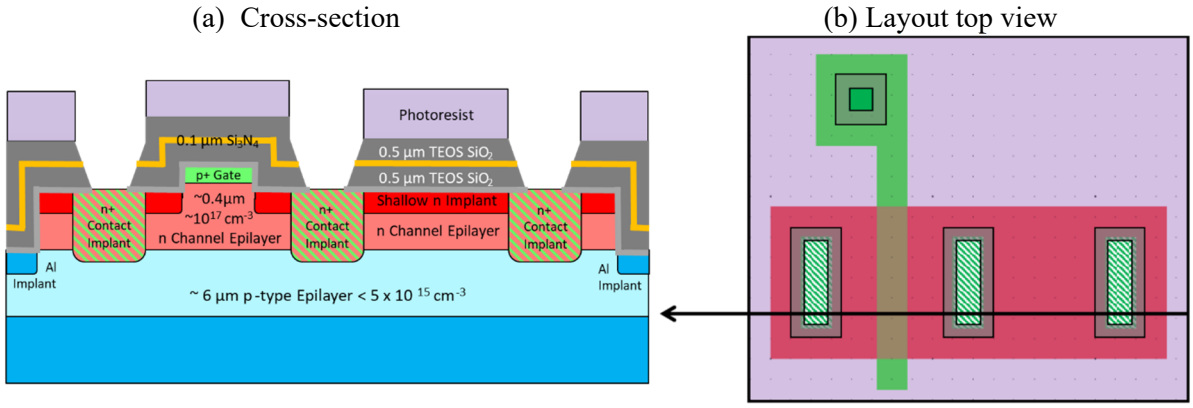

Figure 4: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 2 processing.

Major Step 3, Deposition of Ti + $TaSi_2$ contact metal film: The contactor shall implement further processing consisting of Parts A and B that results in intermediary device structure depicted in Figure 5 as follows:

Part A: The contractor shall load the wafer into an ultrahigh vacuum (UHV) sputter-deposition system equipped with at least two magnetron sputter guns within 2 hours of the completion of Major Step 2. The ultrahigh vacuum chamber shall pumpdown to base pressure less than 5e-7 torr with the wafer at room temperature.

Part B: The contractor shall sputter-deposit using Argon a 20 nm ± 2 nm thickness of 99.999% purity titanium (Ti) film across the wafer surface, which shall be immediately followed (within 20 minutes without breaking vacuum) by sputter-deposition using Krypton a 50 nm ± 5 nm thickness of $TaSi_2$.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 3: Optical microscope images showing a few SiC JFET and resistor mesas recorded after Part B.

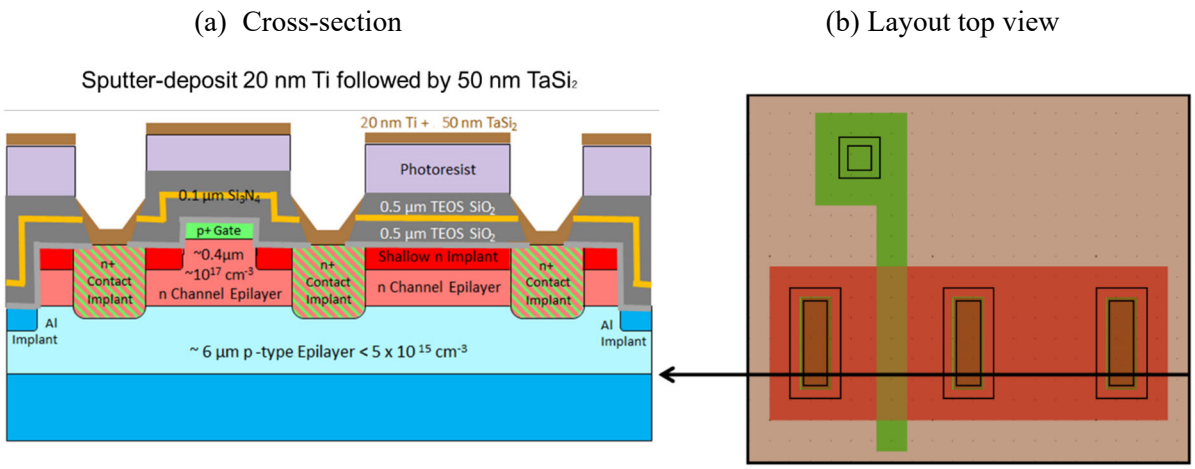

Figure 5: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 3 processing.

Major Step 4, Lift-off patterning of Ti+$TaSi_2$ contact metal film: The contactor shall implement further processing consisting of Parts A and B that results in intermediary device structure depicted in Figure 6 as follows:

Part A: The contractor shall remove all Ti+$TaSi_2$ metal film that was deposited on top photoresist while leaving in place all Ti+$TaSi_2$ metal film that was deposited into Via1 etched regions by dissolving the photoresist to "liftoff" pattern the Ti+$TaSi_2$ metal contact film.

Part B: The contractor shall perform an O_2 plasma clean to ensure complete removal of residual photoresist without removal of any depth of metal or oxide films residing on the wafer.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 4: Optical microscope images showing a few SiC JFET and resistor mesas.

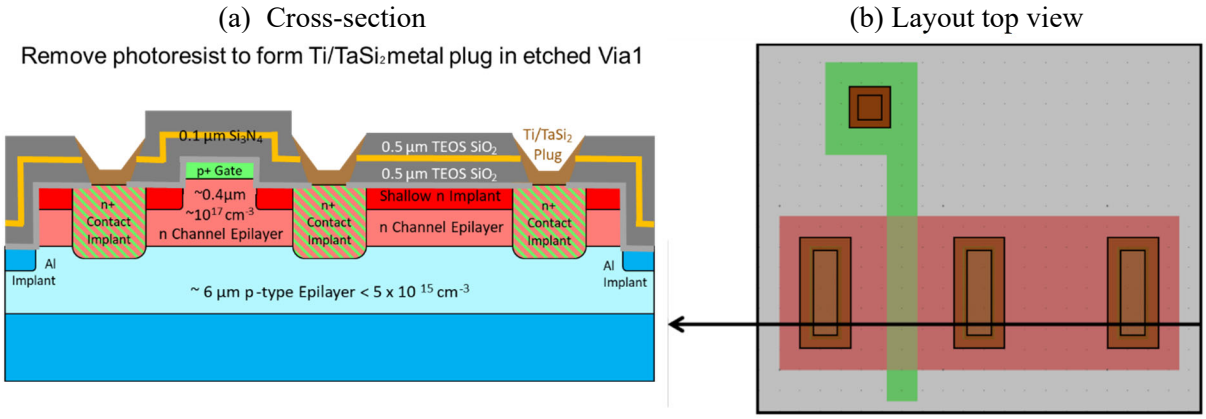

Figure 6: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 4 processing.

Major Step 5, Deposition of 0.7µm $TaSi_2$ Metal1 film: The contractor shall sputter-deposit 0.7µm ± 0.05µm thickness of $TaSi_2$ using Krypton over the entire wafer top surface that results in the intermediary device structure depicted in Figure 7. The resulting $TaSi_2$ film shall exhibit conformal and continuous coverage over all topographic features up to 2 µm in height on the wafer surface.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 5: Optical microscope images showing a few SiC JFET and resistor mesas.

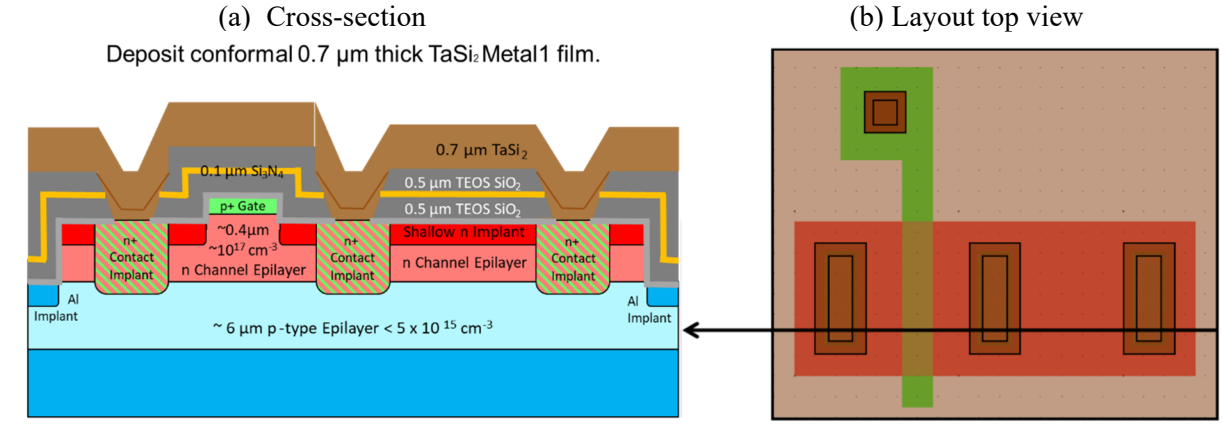

Figure 7: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 5 processing.

Major Step 6, Etching of Metal1 pattern: The contactor shall implement further processing consisting of sequential Parts A, B and C that results in intermediary device structure depicted in Figure 8 as follows:

Part A: The contractor shall implement photolithographic process patterning of a suitable photoresist etch masking material that reproduces the "Metal1" layer pattern in the NASA-provided GDS design file onto the wafer. The NASA-provided design file for this Metal1 pattern has a minimum feature width of 6 µm and a minimum feature separation spacing distance of 6 µm. This Metal1 etch mask shall be deposited and patterned in a manner that aligns to and covers p+ gate features

produced on the wafer during to within 0.2 µm. The reproduced and resulting "Metal1" etch masking pattern defined onto the wafer shall not laterally deviate from the NASA-provided design file dimensions by more than 0.2 µm for 999 out of every 1000 6 µm Metal1 features patterned into the photoresist. The thickness and composition of the photoresist Metal1 mask shall be sufficiently durable that it can remain on the wafer and provide for dry etch removal of the entire thickness of Metal1 film in regions not covered by photoresist during Part B.

Part B: The contractor shall implement plasma-based dry etch removal of the entire 0.7 µm thickness of Metal1 $TaSi_2$ film deposited in Part A across the wafer in those regions where patterned photoresist is not residing prior to the start of the dry etch. In regions not protected by photoresist where the entire thickness $TaSi_2$ is etched, the contractor shall not etch more than 0.25 µm into the underlying SiO_2 dielectric film.

Part C: Following completion of the etching in Part B, the contractor shall remove all photoresist masking material from the entire top surface area of the wafer without removal of any depth of metal or oxide films residing on the wafer. The contractor shall perform an O_2 plasma clean as the final step in photoresist removal to ensure complete removal of residual photoresist without removal of any depth of metal or oxide films residing on the wafer.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 6:

1. Optical microscope images showing a few SiC JFET and resistor mesas.
2. Stylus profilometer data showing topographic height of patterned metal edge feature.
3. I-V probe-test data showing metal conduction of several NASA-selected diagnostic test structures.
4. I-V probe-test data showing isolation/insulation of separated metal traces of several NASA-selected diagnostic test structures.

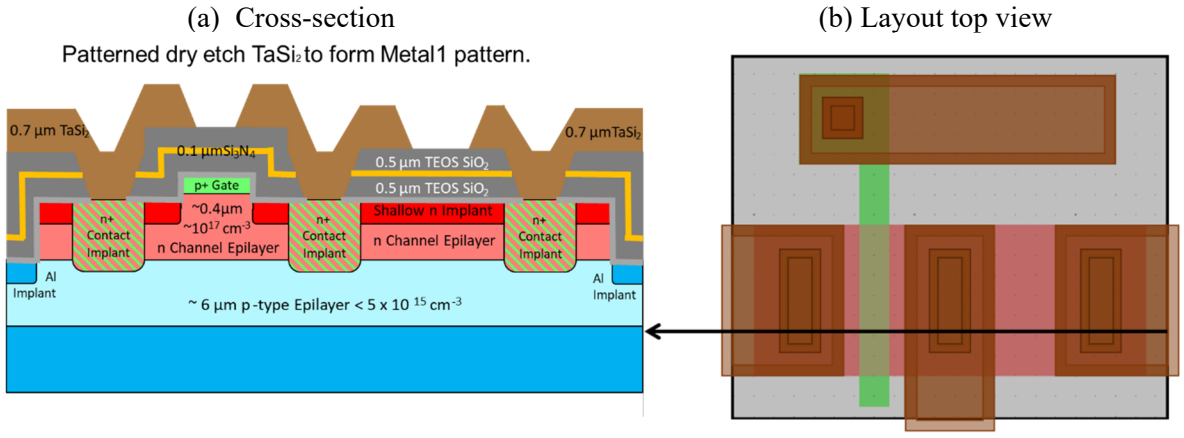

Figure 8: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 6 processing.

Major Step 7, Deposit second 1.1µm-thick 3-layer dielectric stack: The contactor shall implement further processing consisting of Parts A-C that results in intermediary device structure depicted in Figure 9 as follows:

Part A: The contractor shall deposit of 0.5 µm ± 0.05 µm thickness of SiO_2 over the entire wafer top surface. The SiO_2 film shall be deposited by Low Pressure Chemical Vapor Deposition (hereafter abbreviated as LPCVD) using tetraethyl orthosilicate at a deposition temperature of 720 °C. The resulting SiO_2 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

Part B: The contractor shall deposit of 0.1 µm ± 0.01 µm thickness of stoichiometric Si_3N_4 over the entire wafer top surface. The Si_3N_4 film shall be deposited by LPCVD at a deposition temperature of 720 °C. The resulting Si_3N_4 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

Part C: The contractor shall deposit of 0.5 µm ± 0.05 µm thickness of SiO_2 over the entire wafer top surface. The SiO_2 film shall be deposited by LPCVD using TEOS at a deposition temperature of 720 °C. The resulting SiO_2 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 7: Optical microscope images showing a few SiC JFET and resistor mesas.

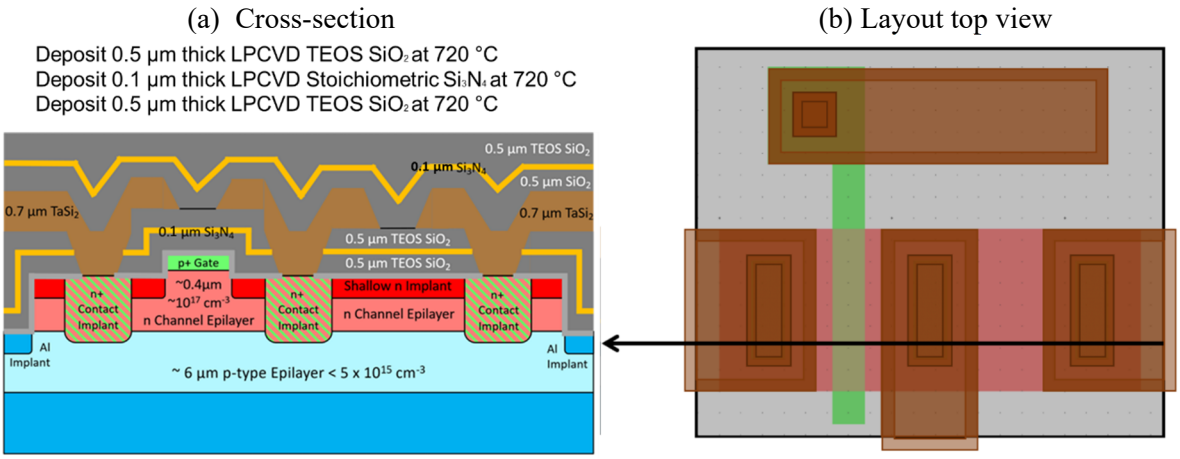

Figure 9: Simplified schematic illustration detail showing (a) respective cross-sections and (b) layout top view of a device region on a wafer following Major Step C-13 processing.

Major Step 8, Photolithography and etching of Via2: The contactor shall implement further processing consisting of Parts A and B that results in intermediary device structure depicted in Figure 10 as follows:

Part A: Implement photolithographic process patterning of a suitable photoresist etch masking material that reproduces the "Via2" layer pattern in the NASA-provided GDS design file onto the wafer. The NASA-provided design file for this Via2 pattern has a minimum feature width of 4.5 µm x 4.5 µm. This Via2 etch mask shall be deposited and patterned in a manner that aligns to and covers p+ gate features produced on the wafer during to within 0.2 µm. The reproduced and resulting "Via2" etch masking pattern defined onto the wafer shall not laterally deviate from the NASA-provided design file dimensions by more than 0.2 µm for 999 out of every 1000 4.5 µm x 4.5 µm Via2 features patterned into the photoresist. The thickness and composition of the

photoresist Via2 mask shall be sufficiently durable that it can remain on the wafer and provide for dry etch removal of the entire thickness of dielectrics as specified in Part B.

Part B: Implement plasma-based dry etch removal of the second 1.1 µm-thick 3-layer dielectric stack (deposited in Major Step 7) dielectric removal only occurs in those lateral 4.5 µm x 4.5 µm regions where patterned photoresist is not residing prior to the start of the dry etch. In each 4.5 µm x 4.5 µm region not protected by photoresist, this etch removal of dielectric shall remove all dielectric to form an exposed $TaSi_2$ Metal1 surface region laterally larger than 3 µm x 3 µm, but this etch removal of dielectric shall not remove/etch more than 0.4 µm of depth into the underlying $TaSi_2$ Metal1.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 8:

1. Optical microscope images showing a few SiC JFET and resistor mesas.
2. Stylus profilometer data showing topographic height of patterned metal edge feature.
3. I-V probe-test data showing metal conduction of several NASA-selected diagnostic test structures.

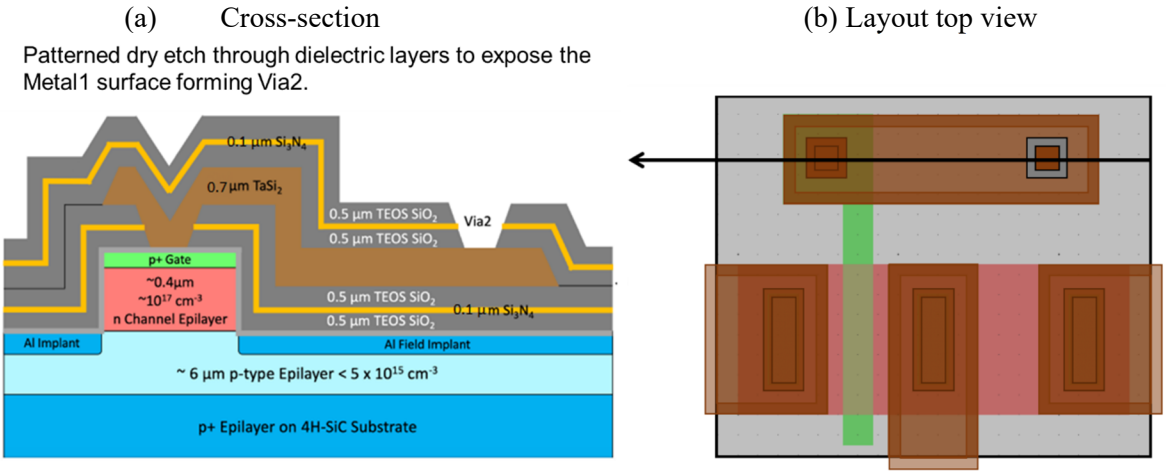

Figure 10: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 8 processing.

Major Step 9, Deposition of 0.7 µm $TaSi_2$ Metal2 film: The contractor shall sputter-deposit using Krypton 0.7 µm ± 0.05µm thickness of $TaSi_2$ over the entire wafer top surface that results in the intermediary device structure depicted in Figure 11. The resulting $TaSi_2$ film shall exhibit conformal and continuous coverage over all topographic features up to 2 µm in height on the wafer surface.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 9: Optical microscope images showing a few SiC JFET and resistor mesas.

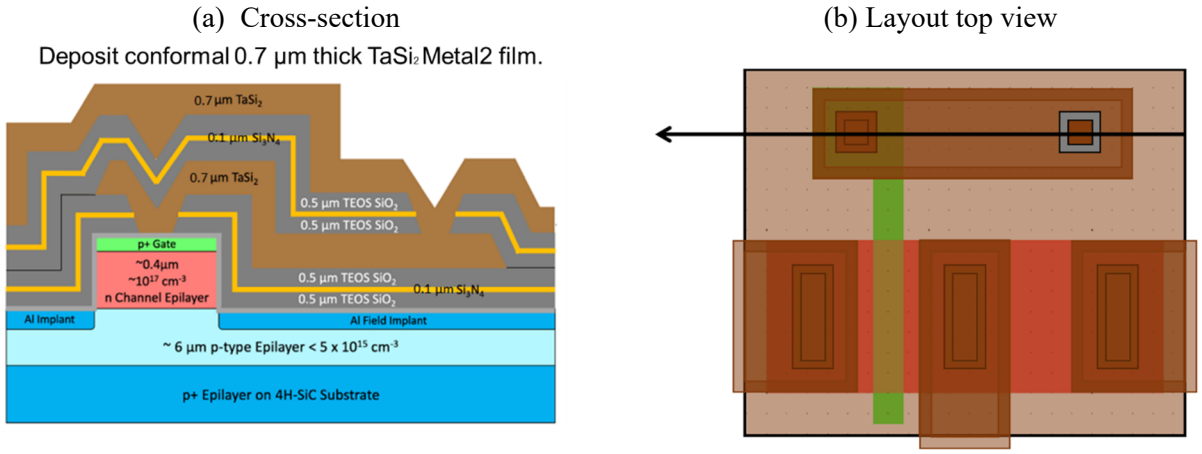

Figure 11: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 9 processing.

Major Step 10, Etching of Metal2 pattern: The contactor shall implement further processing consisting of sequential Parts A, B and C that results in intermediary device structure depicted in Figure 12 as follows:

Part A: The contractor shall implement photolithographic process patterning of a suitable photoresist etch masking material that reproduces the "Metal2" layer pattern in the NASA-provided GDS design file onto the wafer. The NASA-provided design file for this Metal2 pattern has a minimum feature width of 6 µm and a minimum feature separation spacing distance of 6 µm. This Metal2 etch mask shall be deposited and patterned in a manner that aligns to and covers p+ gate features produced on the wafer during to within 0.2 µm. The reproduced and resulting "Metal2" etch masking pattern defined onto the wafer shall not laterally deviate from the NASA-provided design file dimensions by more than 0.2 µm for 999 out of every 1000 6 µm Metal1 features patterned into the photoresist. The thickness and composition of the photoresist Metal2 mask shall be sufficiently durable that it can remain on the wafer and provide for dry etch removal of the entire thickness of Metal2 film in regions not covered by photoresist during Part B.

Part B: The contractor shall implement plasma-based dry etch removal of the entire 0.7 µm thickness of Metal2 $TaSi_2$ film deposited in Part A across the wafer in those regions where patterned photoresist is not residing prior to the start of the dry etch. In regions not protected by photoresist where the entire thickness $TaSi_2$ is etched, the contractor shall not etch more than 0.25 µm into the underlying SiO_2 dielectric film.

Part C: Following completion of the etching in Part B, the contractor shall remove all photoresist masking material from the entire top surface area of the wafer without removal without removal of any depth of metal or oxide films residing on the wafer. The contractor shall perform an O_2 plasma clean as the final step in photoresist removal to ensure complete removal of residual photoresist without removal of any depth of metal or oxide films residing on the wafer.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 10:

1. Optical microscope images showing a few SiC JFET and resistor mesas.
2. Stylus profilometer data showing topographic height of patterned metal edge feature.

3. I-V probe-test data showing metal conduction of several NASA-selected diagnostic test structures.
4. I-V probe-test data showing isolation/insulation of separated metal traces of several NASA-selected diagnostic test structures.

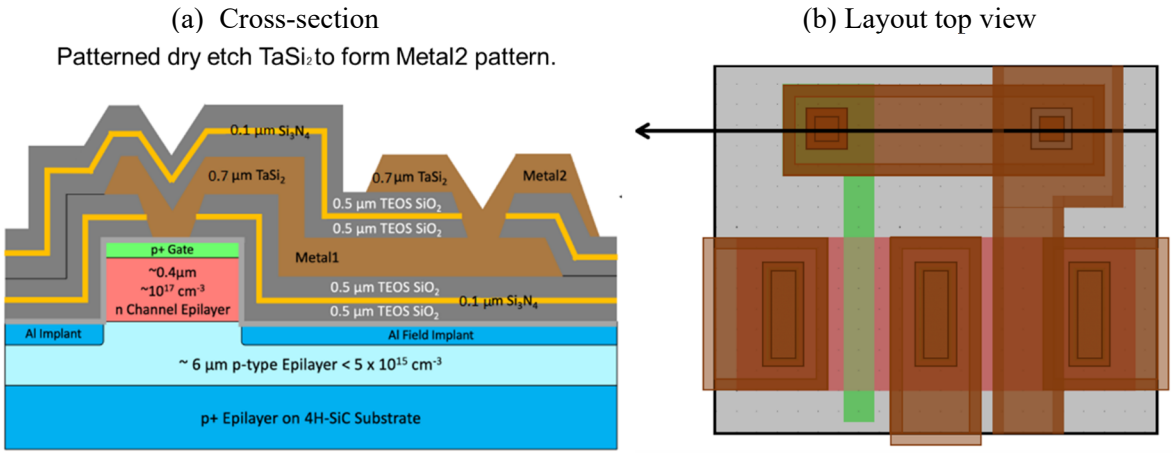

Figure 12: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 10 processing.

Major Step 11, Deposit third 1.7µm-thick 3-layer dielectric stack: The contactor shall implement further processing consisting of Parts A-C that results in intermediary device structure depicted in Figure 13 as follows:

Part A: The contractor shall deposit of 0.8 µm ± 0.08 µm thickness of SiO_2 over the entire wafer top surface. The SiO_2 film shall be deposited by Low Pressure Chemical Vapor Deposition (hereafter abbreviated as LPCVD) using tetraethyl orthosilicate at a deposition temperature of 720 °C. The resulting SiO_2 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

Part B: The contractor shall deposit of 0.1 µm ± 0.01 µm thickness of stoichiometric Si_3N_4 over the entire wafer top surface. The Si_3N_4 film shall be deposited by LPCVD at a deposition temperature of 720 °C. The resulting Si_3N_4 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

Part C: The contractor shall deposit of 0.8 µm ± 0.08 µm thickness of SiO_2 over the entire wafer top surface. The SiO_2 film shall be deposited by LPCVD using TEOS at a deposition temperature of 720 °C. The resulting SiO_2 film shall have average pinhole density less than 1 cm^{-2} across more than 90% of the total top wafer surface area.

The following data/documentation shall be submitted to NASA TM after completion of Major Step 11: Optical microscope images showing a few SiC JFET and resistor mesas.

(a) Cross-section (b) Layout top view

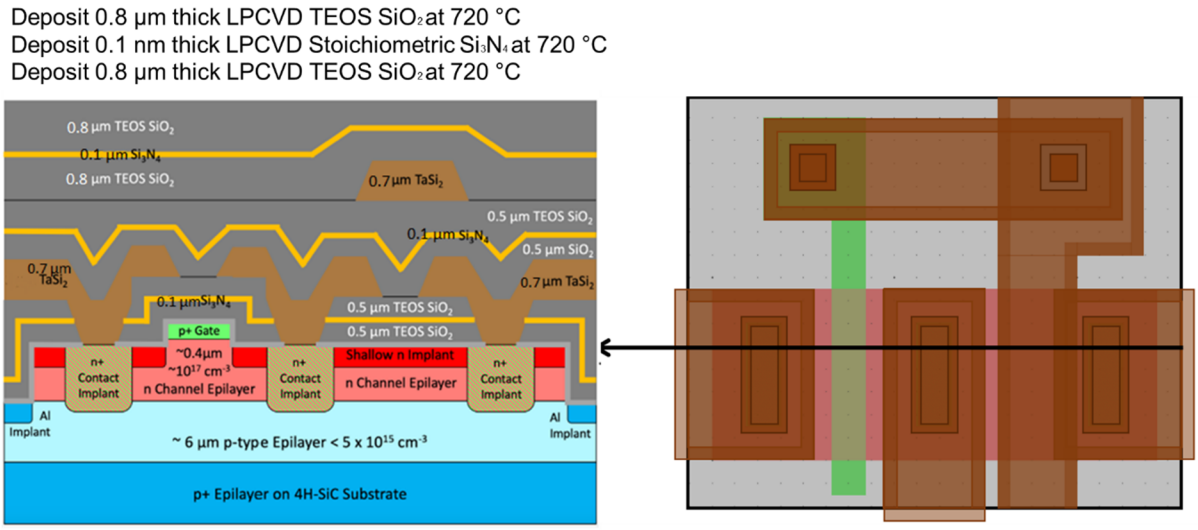

Figure 13: Simplified schematic illustration detail showing (a) cross-section and (b) layout top view of a device region on a wafer following Major Step 11 processing.